WHAT IS CLAIMED IS:

1. A RAM store having a shared SA structure, comprising:

sense amplifiers (SA) arranged in SA strips between two respective adjacent cell blocks for use by a plurality of bit line pairs from the adjacent cell blocks, wherein the bit line pairs have respective charge equalization circuits individually associated with them for the purpose of performing charge equalization between bit line halves of the bit line pairs in a precharge phase; and

a shorting transistor that, when prompted by a control signal, connects the bit line halves of the bit line pairs that are in the precharge phase to one another, wherein the shorting transistor is arranged in or on the respective sense amplifier jointly for all bit line pairs.

2. The RAM store as in claim 1, wherein the shorting transistor can be connected to a respective sense amplifier, and it can be switched by a separate shorting control signal (EQLx) via a dedicated control line.

3. The RAM store as in claim 1, wherein

a respective sense amplifier can be connected to a respective one of two bit line pairs from a left-hand and a right-hand adjacent cell block.

4. The RAM store as in claim 1,

wherein a respective sense amplifier can be connected to a respective one of four bit lines pairs from a left-hand and a right-hand adjacent cell block.

5. The RAM store as in claim 1, wherein the separate shorting control signal supplied via the control line dedicated to the shorting transistors switches all of the shorting transistors in an SA strip.

6. A method for controlling a RAM store having the design of a shared SA structure, in which sense amplifiers arranged in SA strips between two respective adjacent cell blocks are respectively used by a plurality of bit line pairs from the adjacent cell blocks, comprising:

generating a connection control signal separately for each of the bit line pairs associated with the same sense amplifier for connecting the sense amplifier to the respective bit line pair actuated by the connection control signal; and

generating a precharge control signal for performing charge equalization between the bit line halves of the bit line pairs associated with the same sense amplifier in a precharge phase,

wherein the bit line halves of the bit line pairs associated with the same sense amplifier are shorted, when these bit lines pairs are in the precharge phase on account of the precharge control signal supplied to them, by means of a shorting transistor arranged in or on each sense amplifier by supplying this shorting transistor with a dedicated shorting control signal.

7. The control method for a RAM store as in claim 6, wherein in the activation phase for a particular bit line pair, the latter's precharge control signal and the shorting control signal that is supplied to the shorting transistor are deactivated and only the connection control signal for this bit line pair is activated, and

wherein in the precharge phase that comes directly after this activation phase and in which none of the bit line pairs associated with the sense amplifier has been activated, the

connection control signals for connecting the bit line halves of all bit line pairs associated with this sense amplifier are generated and the shorting transistor is supplied with the shorting control signal, and the bit line halves of all of these bit line pairs are supplied with a center level.

8. The control method for a RAM store as in claim 6, wherein for a redundancy design, in which a faulty bit line pair is replaced by a redundant bit line pair, both the precharge control signal for the intact bit line pair and the shorting control signal supplied to the shorting transistor are deactivated in the activation phase for an intact bit line pair among the bit line pairs associated with the same sense amplifier and only the connection control signal is activated, and, in the precharge phase which follows this activation phase and in which none of the bit line pairs associated with this sense amplifier has been activated, the connection control signal is activated exclusively for the previously activated, intact bit line pair up until the next activation command on the same bank, the shorting control signal for the shorting transistor is activated and the bit line halves of all bit line pairs associated with this sense amplifier have the same center level applied to them.

9. The control method for a RAM store as in claim 6,

wherein the connection control signal respectively connects one of two bit line pairs from the adjacent cell blocks to the respective sense amplifier in a bit line assessment phase.

10. The control method for a RAM store as in claim 6,

wherein the connection control signal respectively connects one of four bit line pairs from the adjacent cell blocks to the respective sense amplifier in a bit line assessment phase.